Development of the GTS_leaf Trigger_Core & PLB_Cracus IPs

For EXOGAM_2

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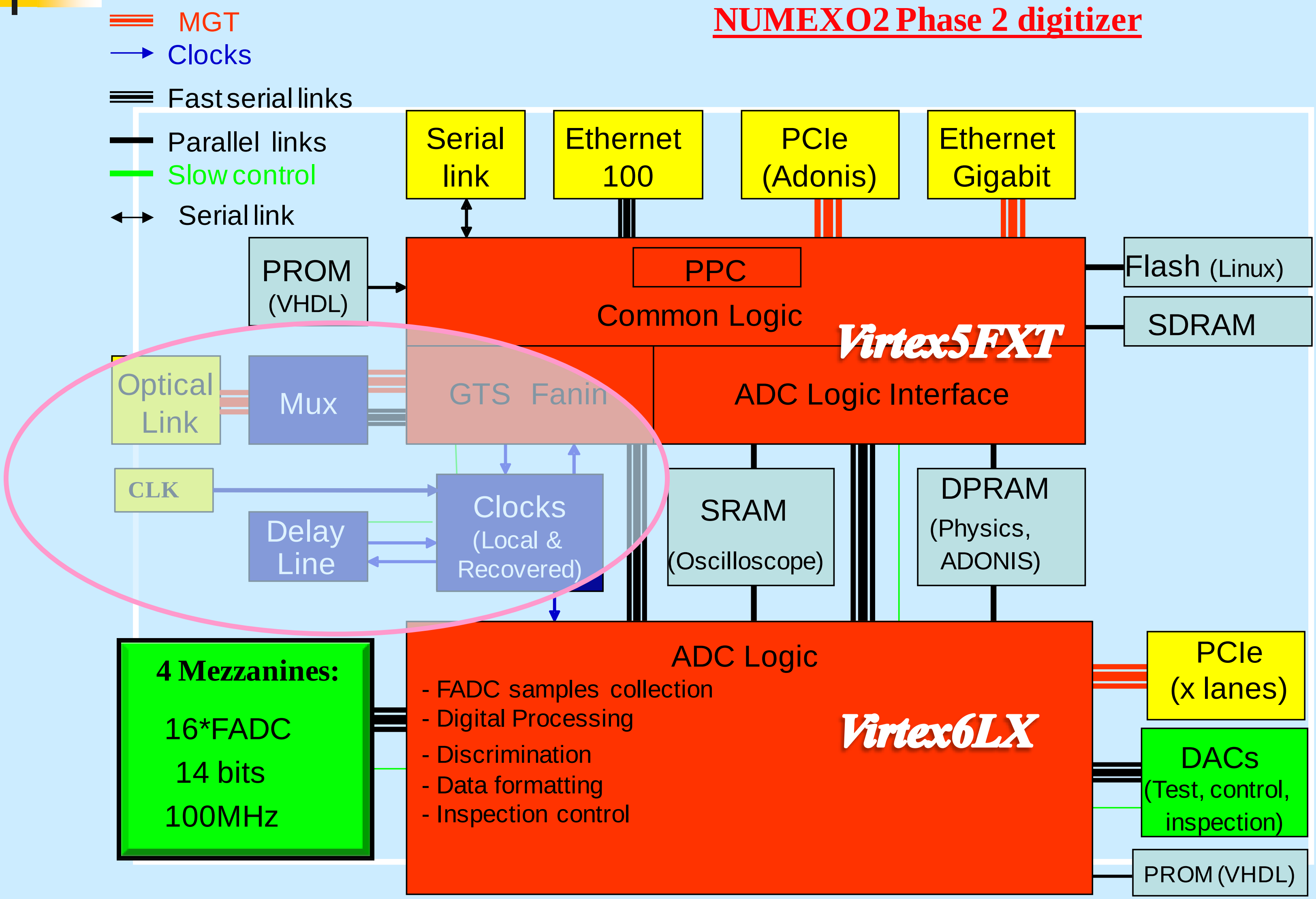
GTS_Leaf Trigger and Synchronization Functions

Type	*Description*
Sampling Synchronization	Synchronization of the detector signals with the clock phase
Serial Link Synchronization	Recovery of parallel data words from the serial bit stream.
Trigger Requests Alignment	Alignment of trigger data at the input of the trigger pipeline processor
L1 Validations Synchronization	Synchronization of L1A signal with data in the readout pipelines
Event Synchronization	Assignment of global clock and event number to data fragments in the DAQ path

NUMEXO2

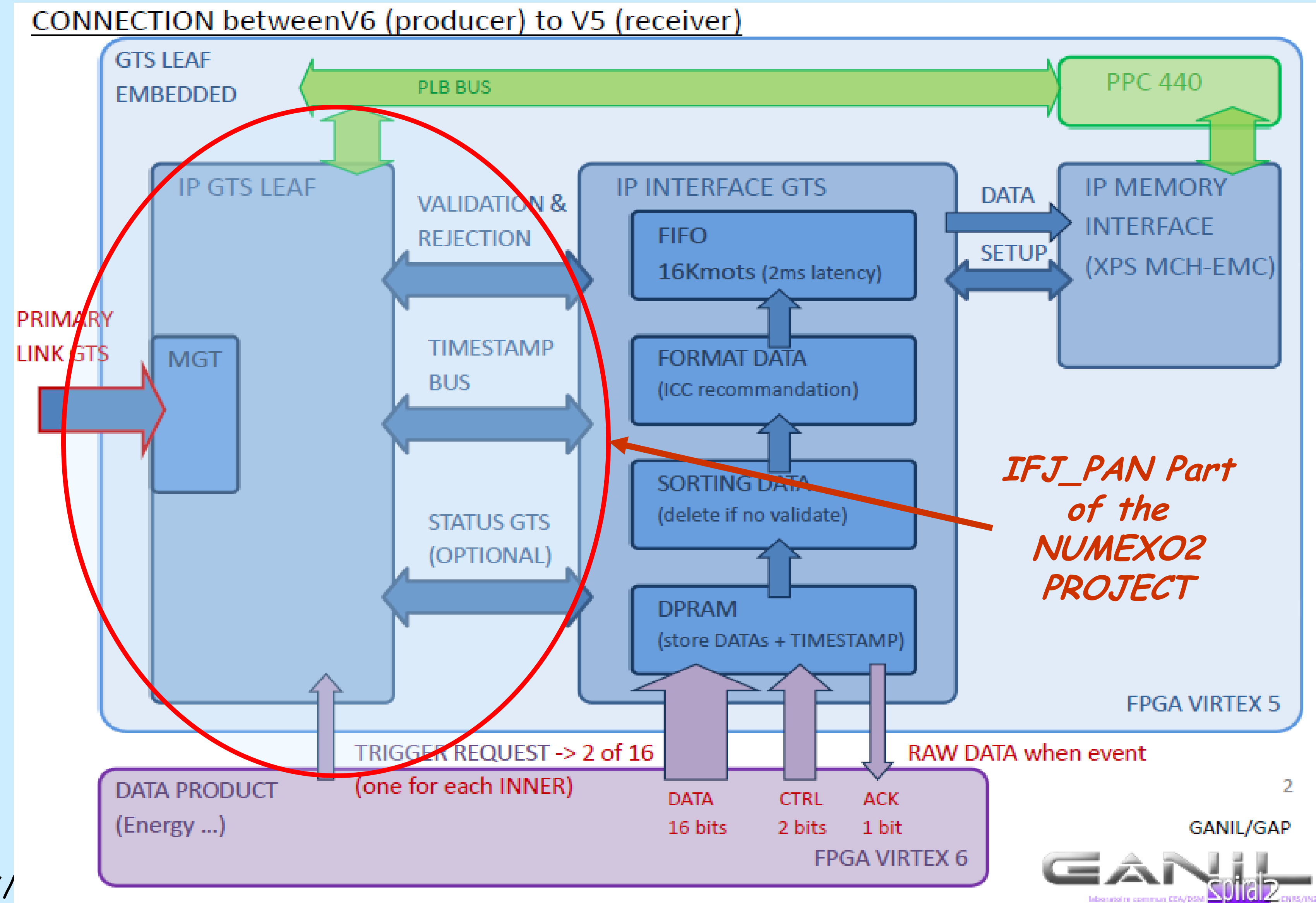
NUMEXO2 Phase 2 digitizer



GTS Functionalities

- 1. common clock → 100 MHz
- 2. global clock counter 48 bit
- 3. global event counter 16 bit
- 4. trigger controls:
  - **i. Throttling of the L1 validation signal**
  - **ii. Fast commands (fast reset, initialization, etc.)**
  - **iii. Fast monitoring feedback from the detector elements**
  - **iv. Calibration and test trigger sequence commands**
  - **v. Monitor of dead time**
- 5. Trigger requests
- 6. Error reports Abnormal conditions

IFJ PAN task



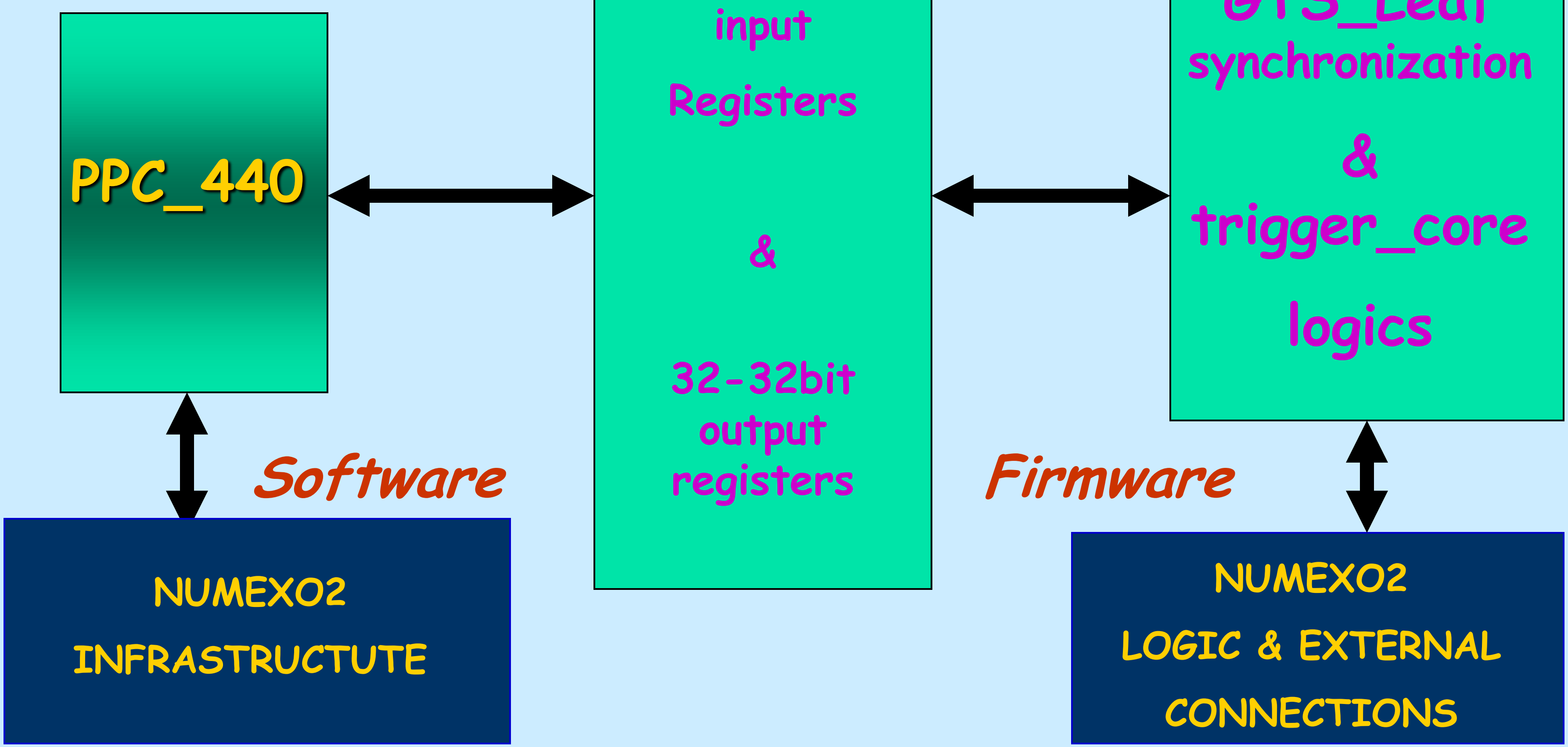
CONNECTION betweenV6 (producer) to V5 (receiver)
GTS LEAF
EMBEDDED
PLB BUS
PPC 440
IP GTS LEAF
VALIDATION &
REJECTION
IP INTERFACE GTS
DATA
SETUP
IP MEMORY
INTERFACE
(XPS MCH-EMC)
FIFO
16Kmots (2ms latency)
PRIMARY
LINK GTS
MGT
TIMESTAMP
BUS
FORMAT DATA
(ICC recommandation)
SORTING DATA
(delete if no validate)
IFJ_PAN Part
of the
NUMEXO2
PROJECT
STATUS GTS
(OPTIONAL)
DPRAM
(store DATAs + TIMESTAMP)
FPGA VIRTEX 5
TRIGGER REQUEST -> 2 of 16
(one for each INNER)
RAW DATA when event
DATA PRODUCT
(Energy ...)
DATA
16 bits
CTRL
2 bits
ACK
1 bit
FPGA VIRTEX 6
2
GANIL/GAP

GTS_Leaf logic on Virtex_5 (xc5vfx70t)

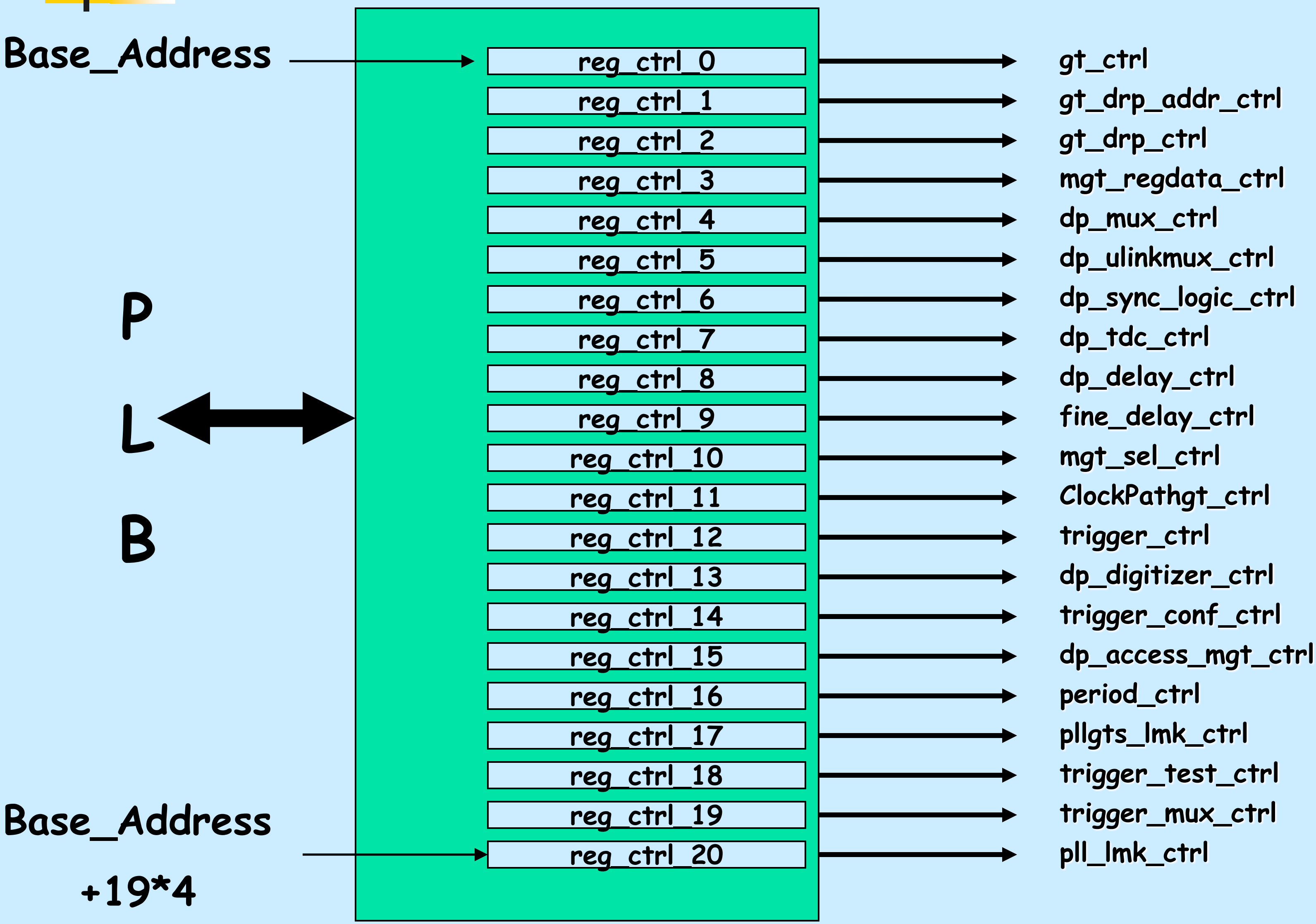
Plb_cracus IP

Form INTERFACE between

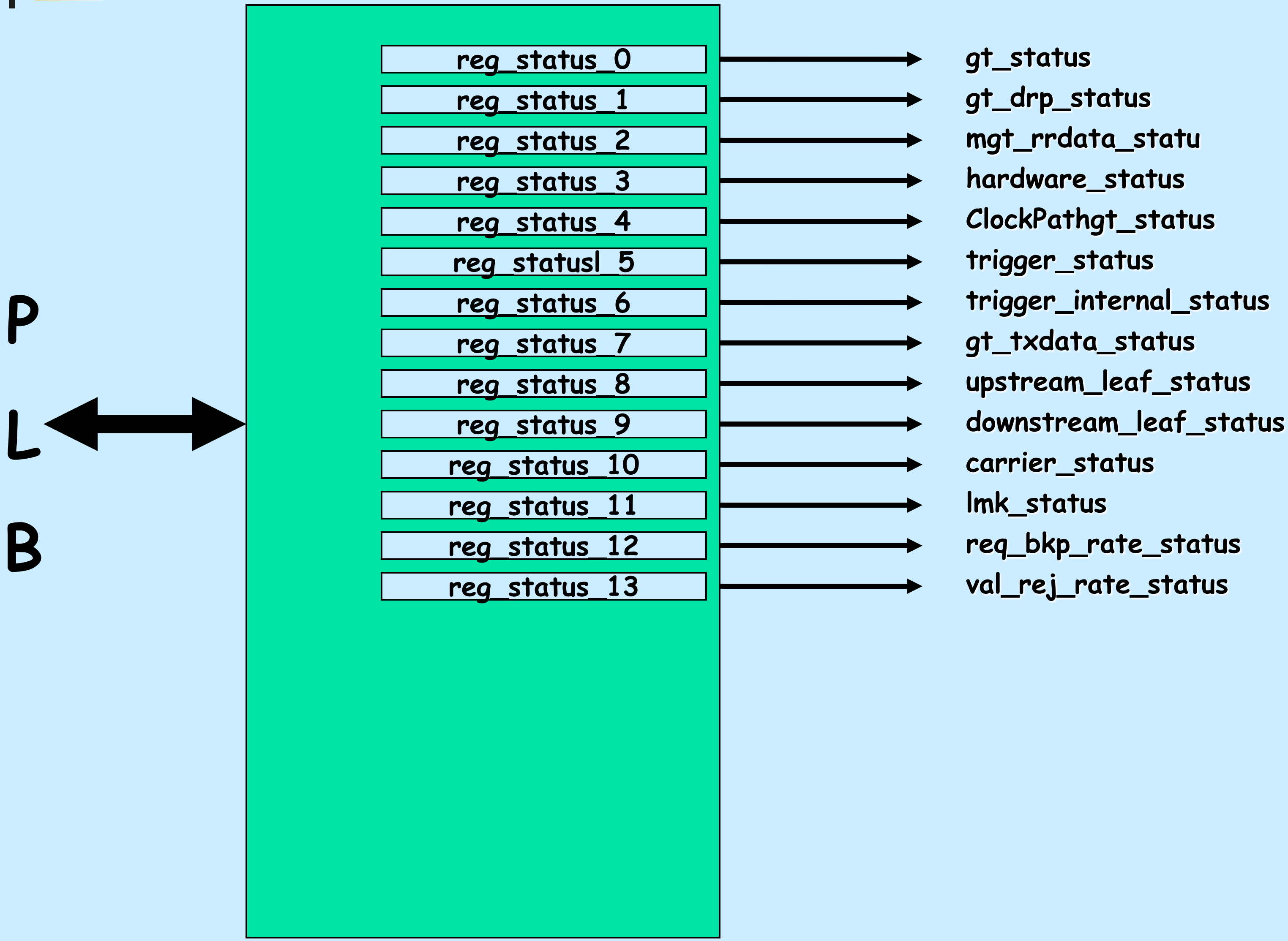
PPC_440 ⇔ GTS_Leaf



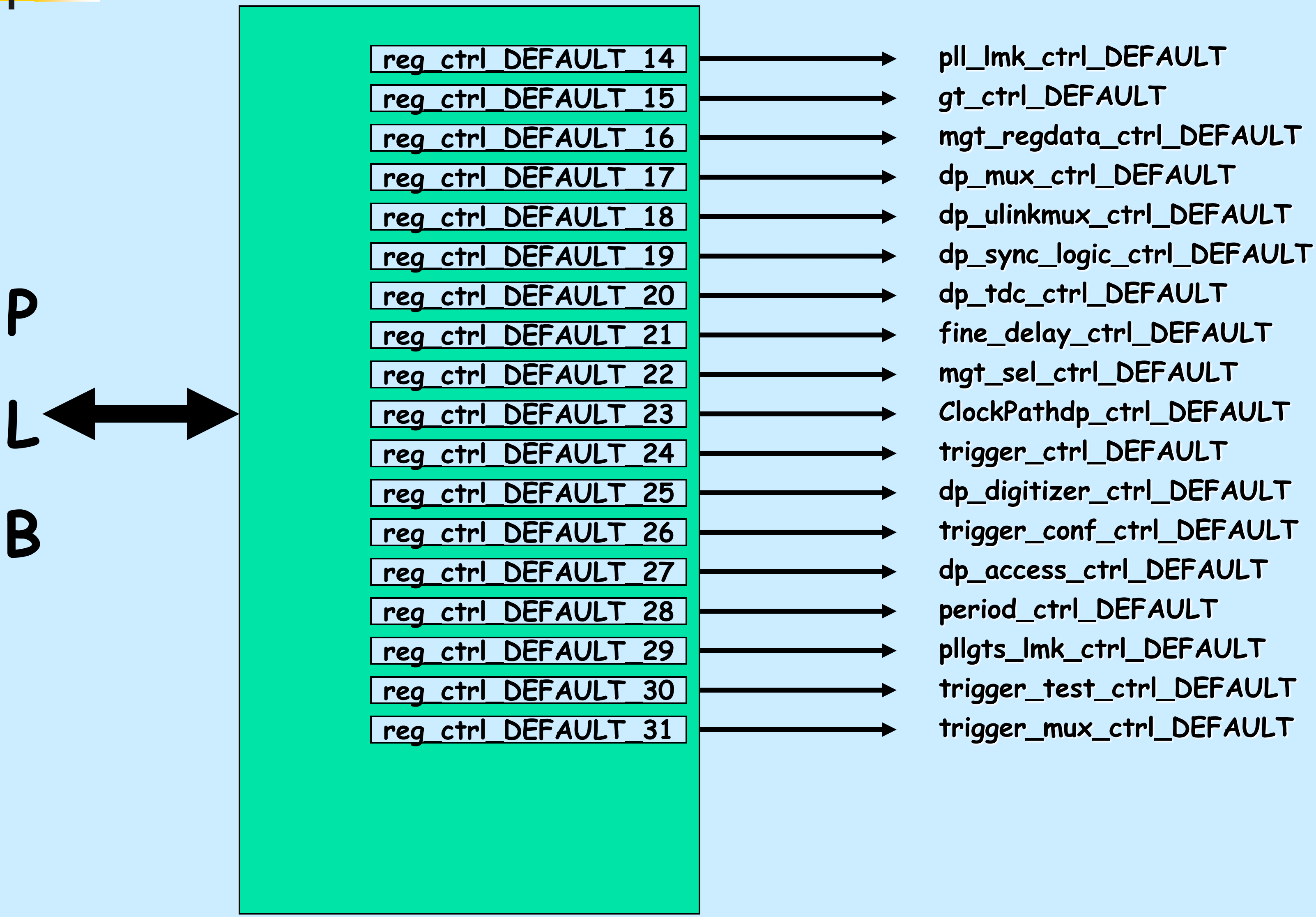
plb_cracus ctrl_registers



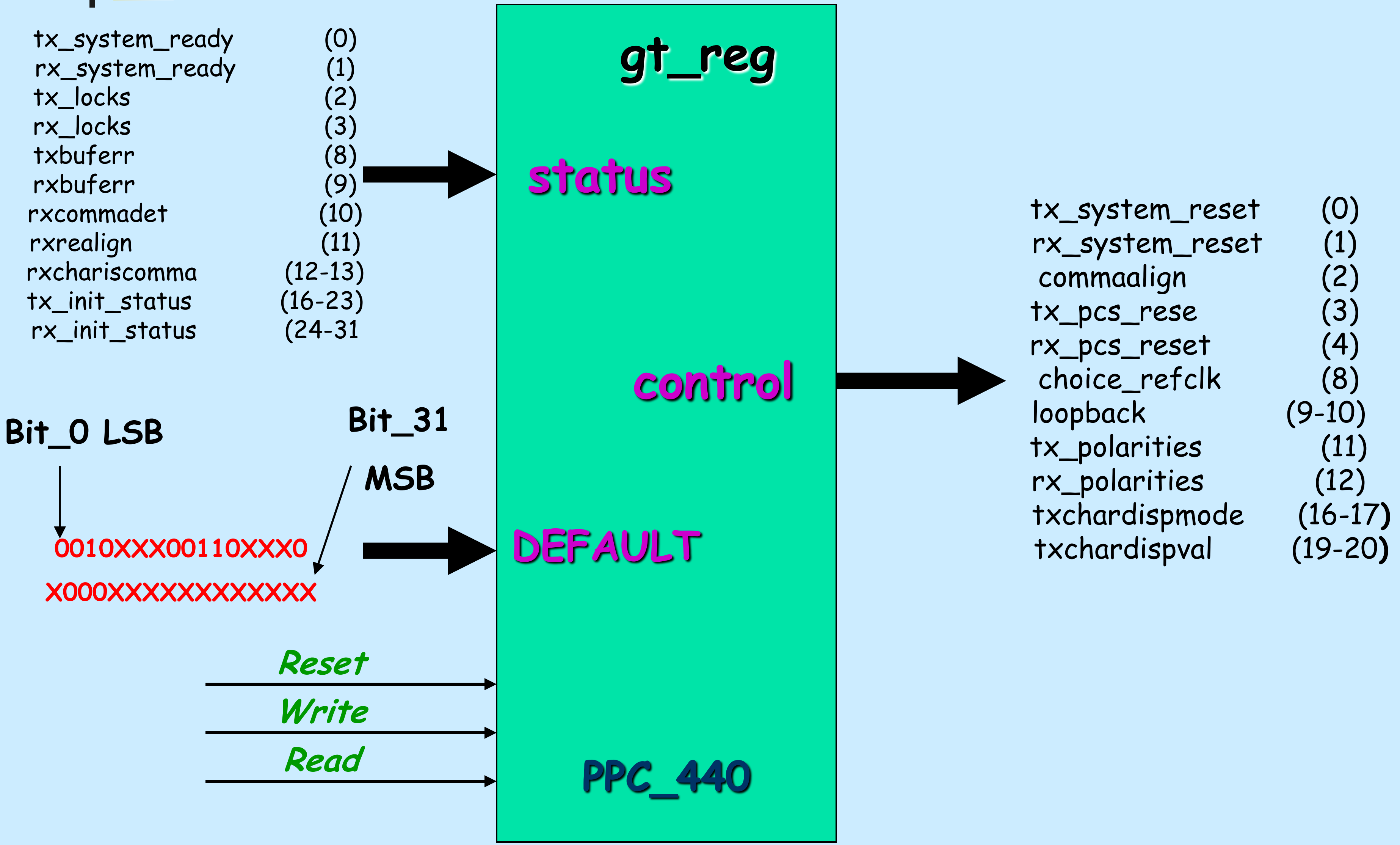
plb_cracus status_registers



plb_cracus ctrl_DEFAULT_registers



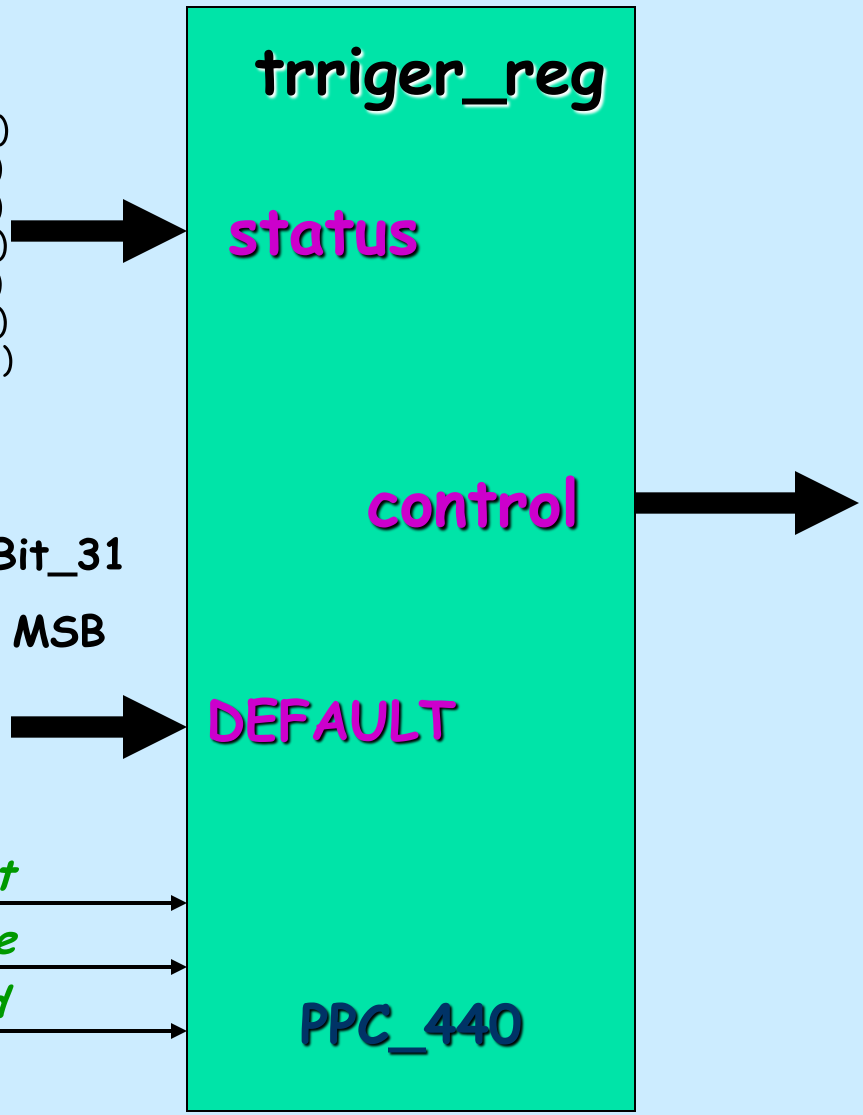
gt_register



tx_system_ready (0)
rx_system_ready (1)
tx_locks (2)
rx_locks (3)
txbuferr (8)
rxbuferr (9)
rxcommadet (10)
rxrealign (11)
rxchariscomma (12-13)
tx_init_status (16-23)
rx_init_status (24-31
gt_reg
status
control
DEFAULT
PPC_440
Bit_0 LSB
Bit_31
MSB
0010XXX00110XXX0
X000XXXXXXXXXXXX
Reset
Write
Read
tx_system_reset (0)
rx_system_reset (1)
commaalign (2)
tx_pcs_rese (3)
rx_pcs_reset (4)
choice_refclk (8)
loopback (9-10)
tx_polarities (11)
rx_polarities (12)
txchardispmode (16-17)
txchardispval (19-20)

trigger_register

trigger_type (0-7)
rst (8)
rst_dcm_user (9)
dcm_all_locked (10)
dcm_locked_user (11)
software_rst (12)
leds ? (16-22)



gts_ready (0)
rst_dcm_uP (1)
rst_core_uP (2)
loopback_enable (3)
test_enable (4)
aurrora_loopback (5)
timestamp_enable (6)
reject_window (16-31)

Bit_0 LSB

Bit_31

MSB

1001001XXXXXXXXX
0000010100000000
(12.8 μs for timeout)

Reset
Write
Read

gt_drp_register