GTS_LEAF
Implemetation for Virtex 5

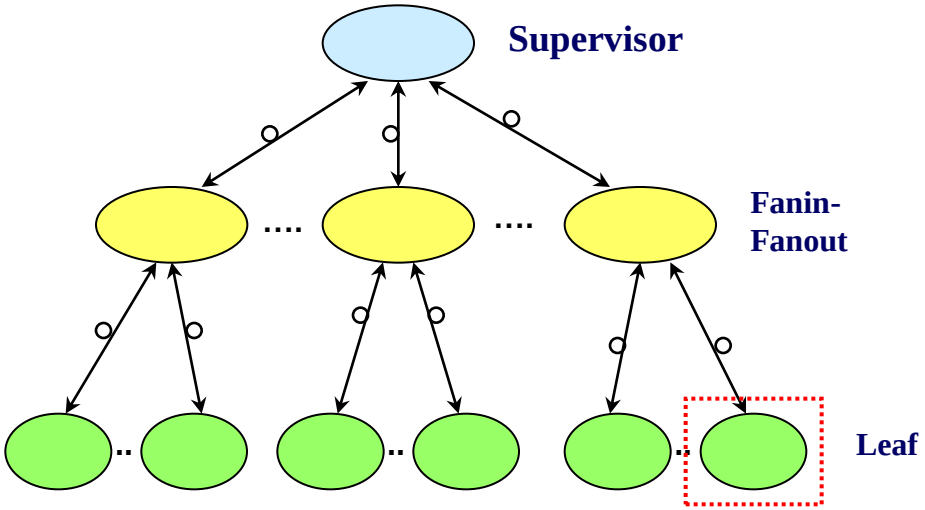
Overview

- GTS topology and functions
- Redesign of GTS for Exogam2 tasks
- E.T.Subramaniam MGT design block diagram
- Block diagram of GTS leaf
- Clock Management
- MGT control
- Trigger Leaf
- Done and to be done

GTS functions and topology

The main functions of the GTS are:

- source of common 100 MHz clock
- provide Time stamp
- provide Event Number
- validate or reject triggers



GTS tree topology

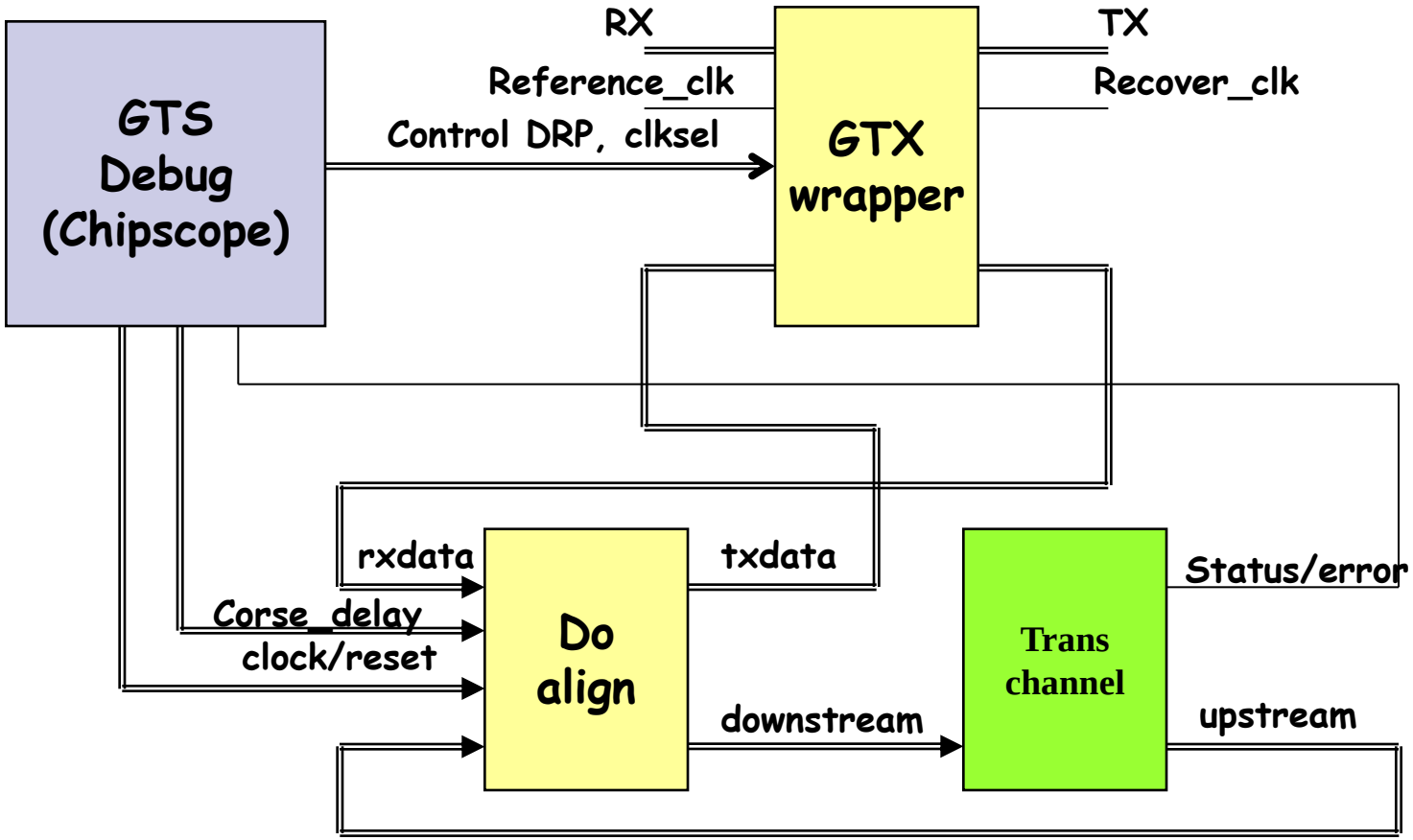
GTS V3 mezzanine with Virtex 4
(Padova design for AGATA)

The NUMEX02 needs only GTS leaf and one MGT

Redesign of GTS firmware for Exogam2 tasks

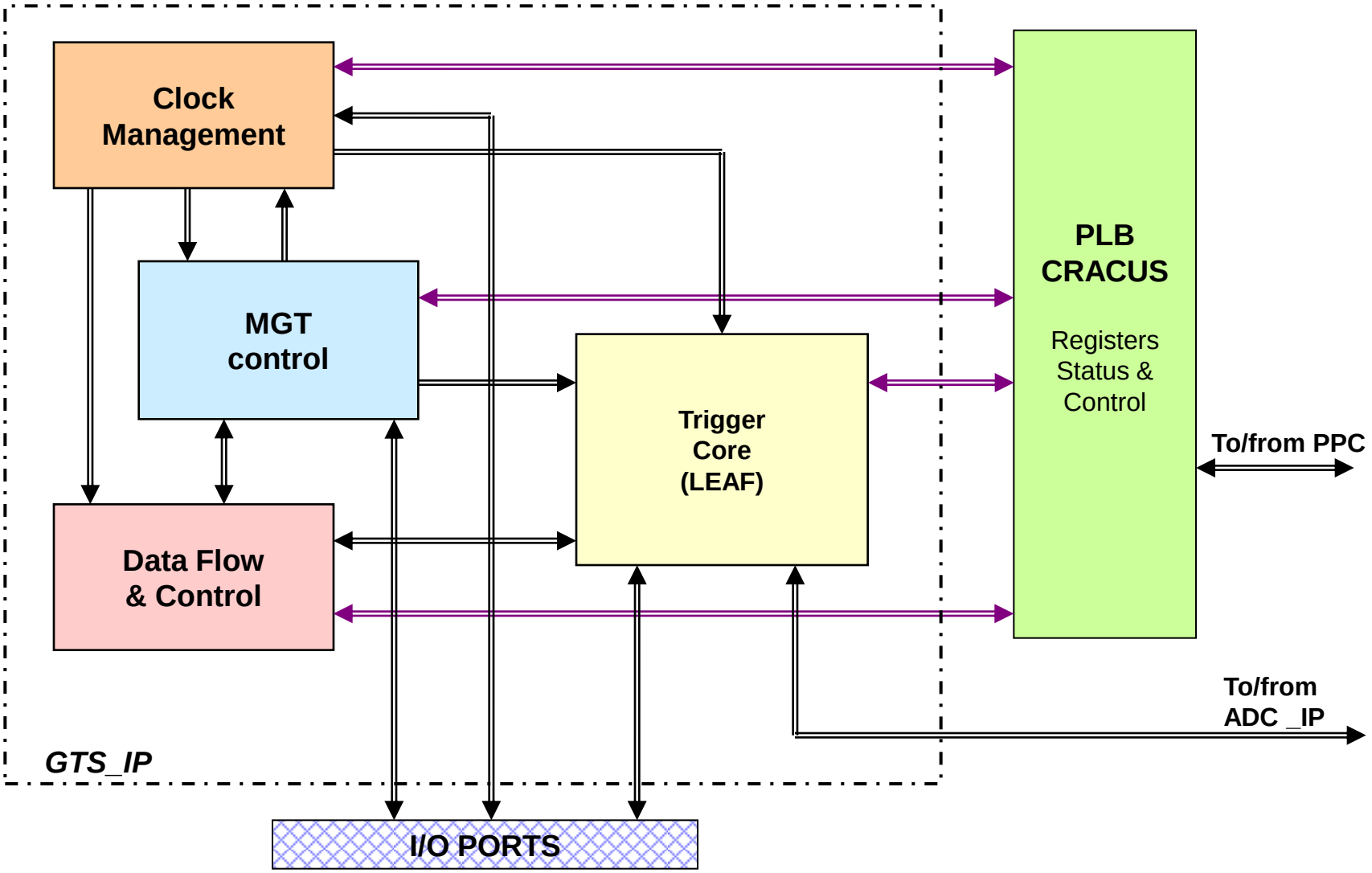
- reduce Trigger core IP to the trigger leaf IP function
- migrate Xilinx library components from Virtex_4 to Virtex_5
- design one MGT of the Vitex_5 with the best possible compatibility to the Virtex_4 Rocket IOs
- redesign the Clock Management to the NUMEX02 specification
- connect the necessary control and status registers to the PLB bus for configurations and debugging purposes, compatible to GTS V3 (PLB_Cracus made by Adam Czermak)
- implement GTS IP in Virtex_5 and test with ML507 card.

E.T.Subramaniam MGT design block diagram

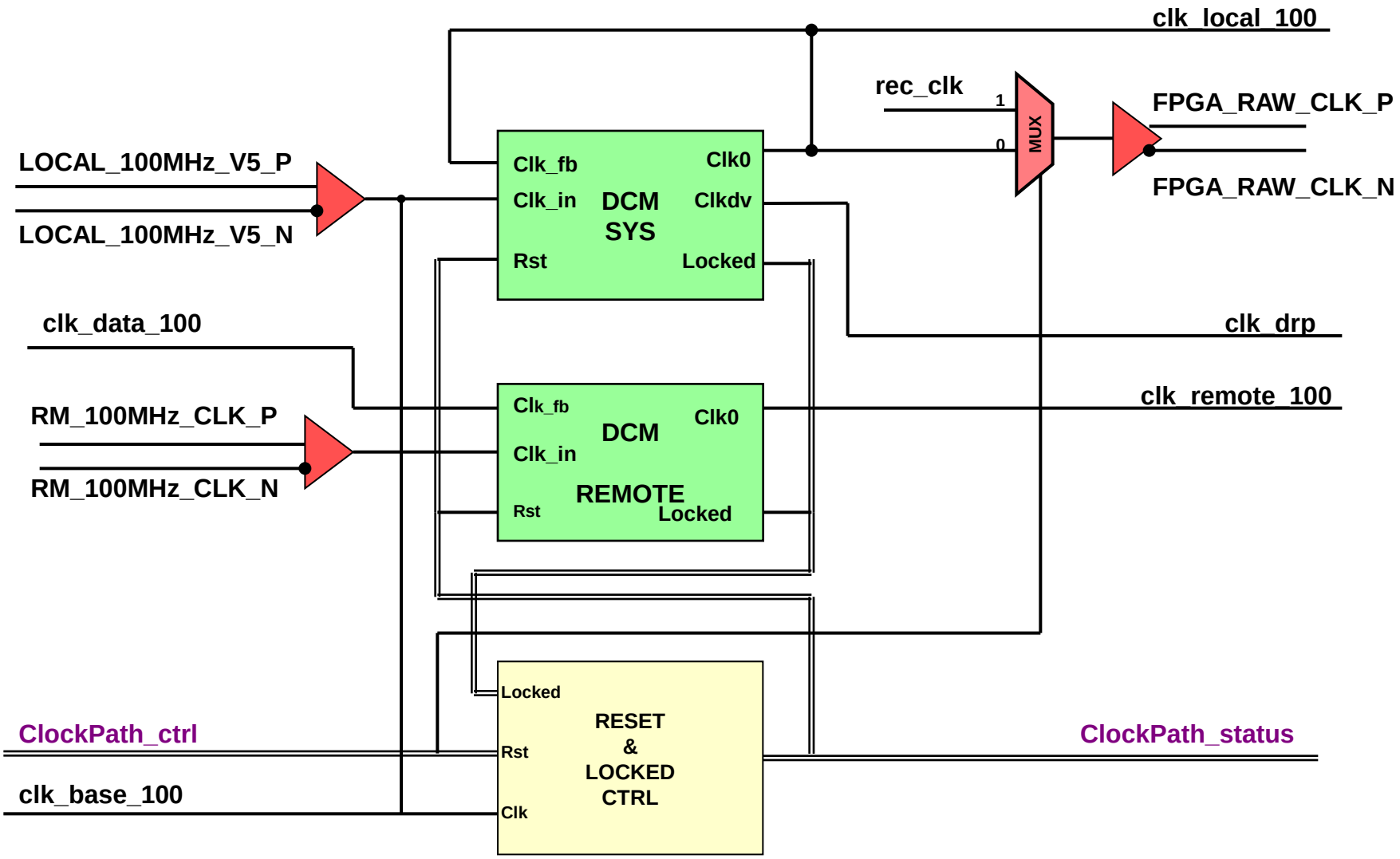


Test: done with ML507

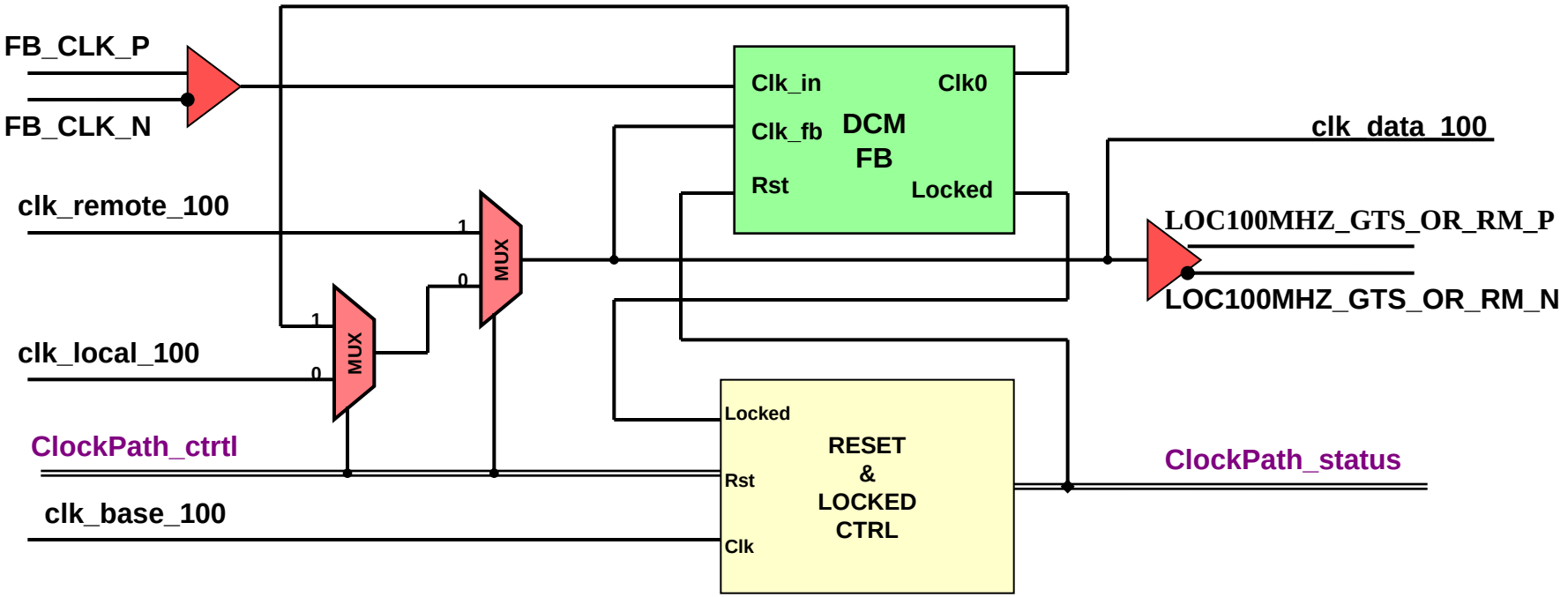
Goal: migration and compatibility of MGT from Virtex_4into Virtex_5 proved

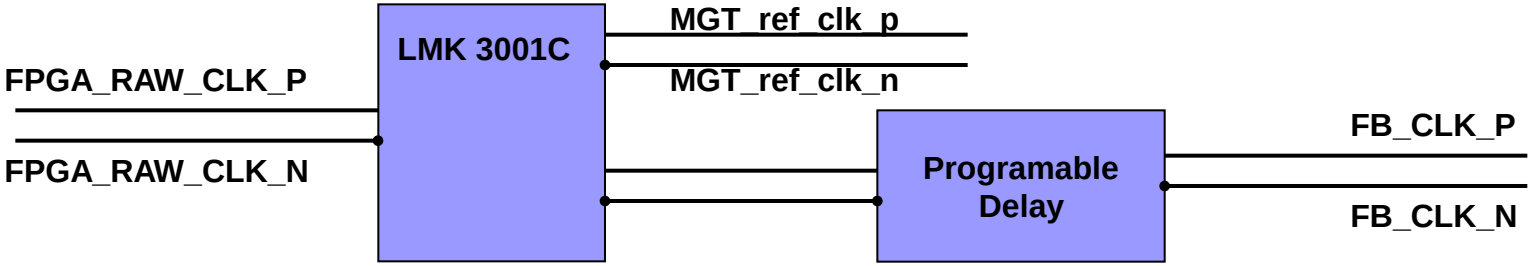


Block Diagram of GTS_IP

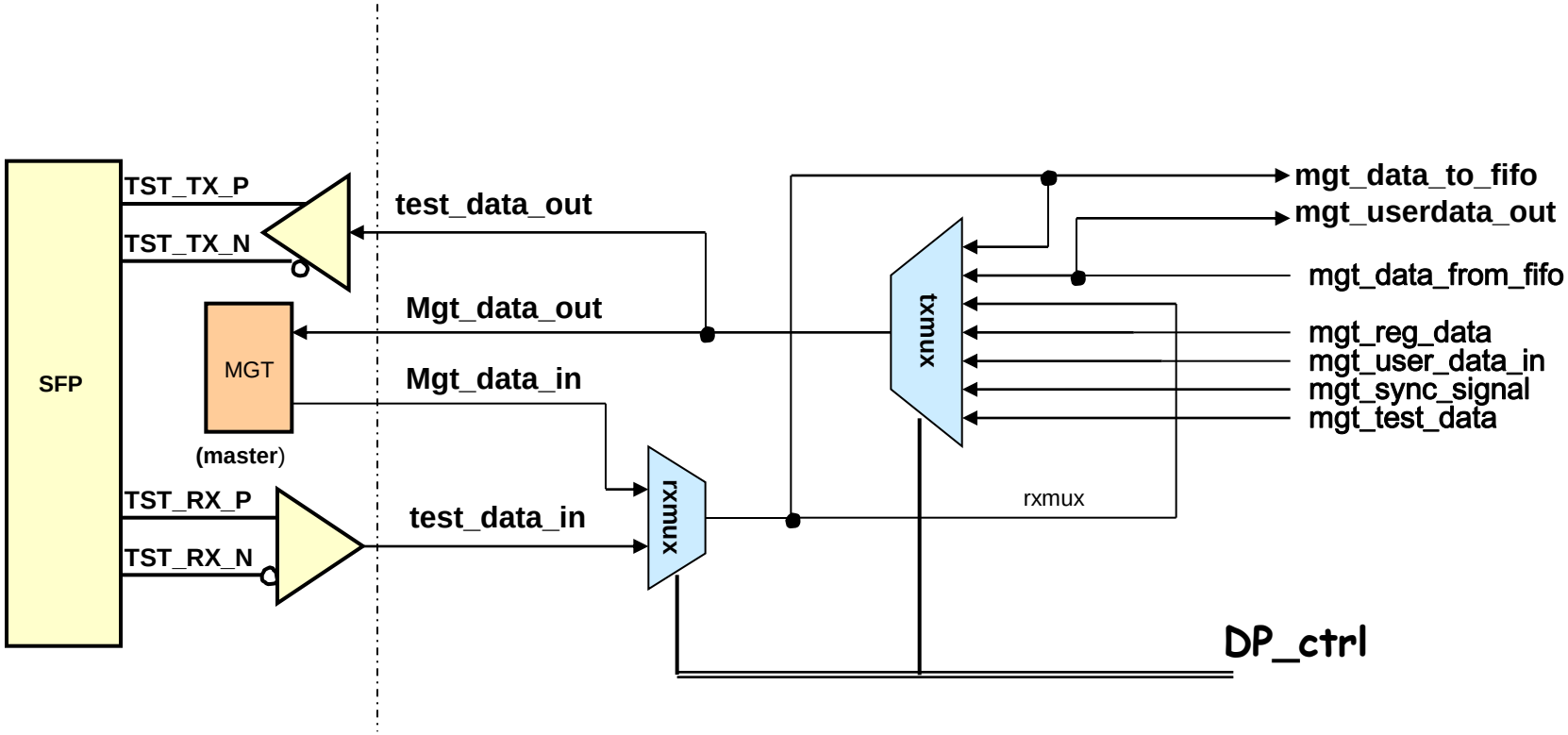


Clock Managment_1. Local & Remote clock

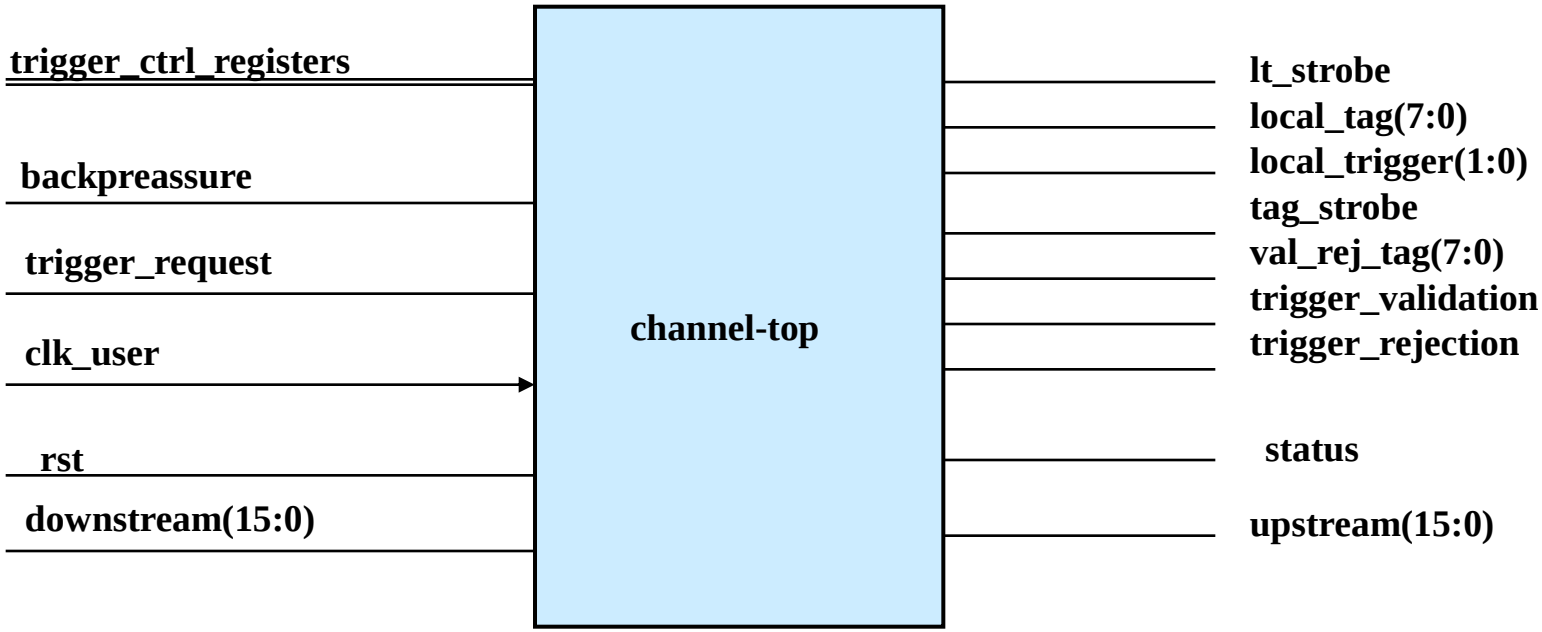




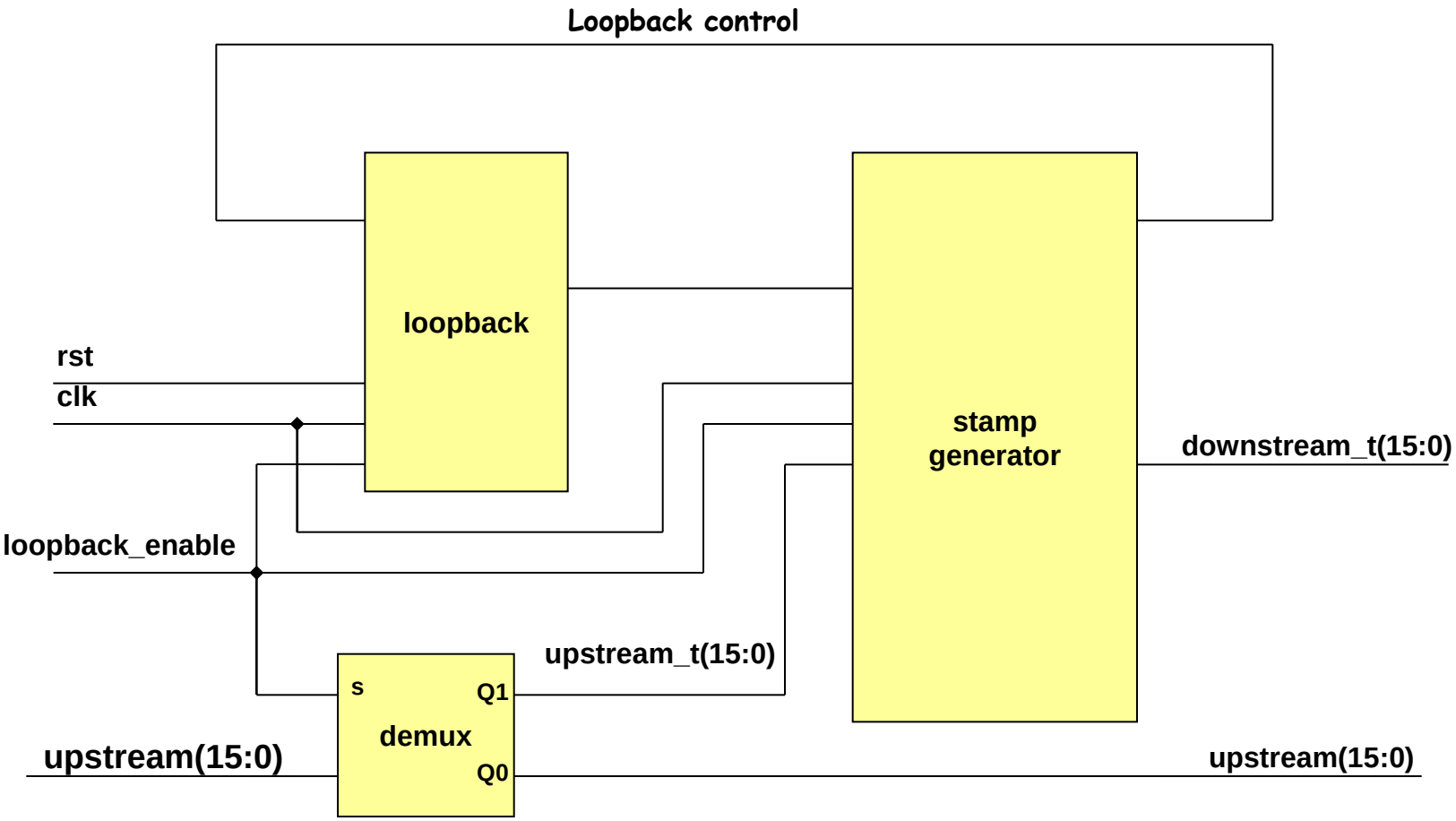
Clock Managment_2. Feedback clock



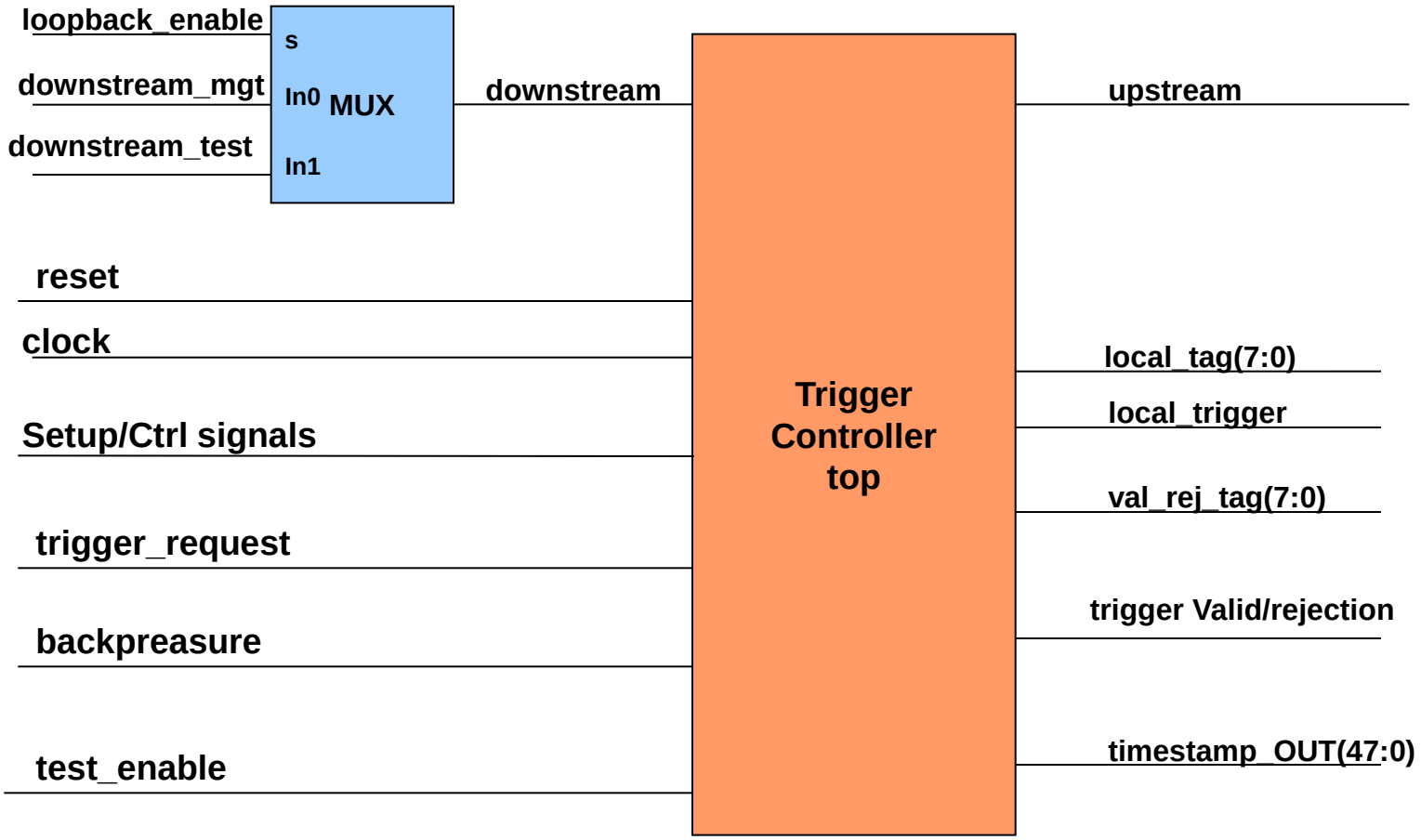
Part of Data Path (for master MGT)



Trigger_leaf



Trigger leaf_1



Trigger leaf_2